IN THE CLAIMS

1. (Currently amended) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks each including a plurality of rows of CAM cells, wherein each CAM array block has a unique hard priority indicative of the CAM array block's physical location relative to the other CAM array blocks, and has an arbitrarily assigned soft priority that is independent of the CAM array block's physical location relative to the other CAM array blocks; and

a priority resolution circuit configured to hierarchically resolve competing soft priorities between a plurality of active hit signals according to numeric significance so that a first of the plurality of active hit signals having a first soft priority will block resolution of a second of the plurality of active hit signals having a second soft priority when the first soft priority is higher than the second soft priority and vice versa when the second soft priority is higher than the first soft priority, and configured to resolve competing hard priorities between two or more of the plurality of active hit signals having equivalent highest soft priorities by identifying which of the two or more of the plurality of active hits signals has the highest hard priority.

2. (Canceled)

3. (Currently amended) The CAM device of Claim 21, wherein said priority resolution circuit comprises a MSB soft priority resolution stage and a LSB soft priority resolution stage.

4. (Previously Presented) The CAM device of Claim 3, wherein said priority resolution circuit comprises a hard priority resolution stage electrically coupled to outputs of said LSB soft priority resolution stage; and wherein said priority resolution circuit is further configured so that competing and unequal soft priorities of at least some of the plurality of active hit signals are completely resolved by the MSB and LSB soft priority resolution stages prior to further resolution of hard priority by the hard priority resolution stage.

5. (Currently amended) The CAM device of Claim 1, ~~further comprising:~~

~~a plurality of CAM array blocks having respective soft priorities assigned thereto;~~

wherein ~~said~~ the priority resolution circuit comprises a plurality of registers that retain the soft priorities assigned to ~~said~~ the plurality of CAM array blocks; and

wherein ~~said~~ the priority resolution circuit is configured so that the soft priorities retained by the plurality of registers can be arranged in any order regardless of the values of hard priorities ~~assigned to said plurality of~~ the CAM array blocks.

6. (Canceled)

7. (Currently amended) The CAM device of Claim 61, wherein ~~said hierarchical~~ the priority resolution circuit is configured to sequentially evaluate the soft priorities of ~~said~~ the plurality of CAM array blocks in descending order according to numeric significance.

8. (Canceled)

9. (Currently amended) The CAM device of Claim 61, wherein ~~said hierarchical~~the priority resolution circuit comprises:

a first soft priority resolution circuit that is electrically coupled in a wired-OR manner to a first plurality of signal lines; and

a second soft priority resolution circuit that is electrically coupled in a wired-OR manner to a second plurality of signal lines.

10. (Original) The CAM device of Claim 9, wherein the first and second plurality of signal lines are floated or biased at precharged levels during the search operation.

11. (Currently amended) The CAM device of Claim 9, wherein ~~said hierarchical~~the priority resolution circuit further comprises:

a third soft priority resolution circuit that is electrically coupled in a wired-OR manner to a third plurality of signal lines.

12. (Currently amended) The CAM device of Claim 11, wherein ~~said hierarchical~~the priority resolution circuit further comprises:

a hard priority resolution circuit that is electrically coupled to outputs of ~~said~~ the third soft priority resolution circuit.

13. (Currently amended) The CAM device of Claim ~~6~~1, wherein ~~said hierarchical~~the priority resolution circuit comprises:

a soft priority resolution circuit; and

a hard priority resolution circuit that is electrically coupled to outputs of ~~said~~ the soft priority resolution circuit.

14. (Currently amended) The CAM device of Claim ~~6~~1, wherein ~~said hierarchical~~the priority resolution circuit comprises:

a soft priority resolution circuit that is electrically coupled in a wired-OR manner to a first plurality of signal lines that are floated or biased at precharged levels during a priority resolution operation; and

a hard priority resolution circuit that is electrically coupled to outputs of ~~said~~ the soft priority resolution circuit.

15-18. (Canceled)

19. (Currently amended) A content addressable memory (CAM) device, comprising:

a priority resolution circuit configured to resolve competing soft priorities between a plurality of active hit signals associated with a corresponding plurality of CAM array blocks, each having a plurality of rows of CAM cells, in order to identify two or more active hit signals having highest equivalent soft priorities and further configured to resolve competing hard priorities between the two or more active hit signals in order to identify one as having the highest hard priority; and

wherein ~~said~~ the priority resolution circuit is configured to resolve the competing soft priorities for all possible combinations of soft priority order between the plurality of active

hit signals, wherein each hard priority is a unique value indicative of the corresponding CAM array block's physical location relative to the other CAM array blocks, and each soft priority is an arbitrarily assigned value that is independent of the corresponding CAM array block's physical location.

20. (Original) The CAM device of Claim 19, wherein the competing soft priorities of the plurality of active hit signals are resolved by evaluating the soft priorities in a MSB to LSB sequence.

21. (Original) The CAM device of Claim 19, wherein said priority resolution circuit is a hierarchical priority resolution circuit having at least two soft priority resolution stages and a hard priority resolution stage.

22. (Currently amended) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks ~~having respective soft priorities assigned thereto~~, each including a plurality of rows of CAM cells, wherein each CAM array block has a unique hard priority indicative of the CAM array block's physical location relative to the other CAM array blocks, and has an arbitrarily assigned soft priority that is independent of the CAM array block's hard priority; ~~and~~

means for identifying a highest priority one of said plurality of CAM array blocks having respective matching entries therein during a search operation, by evaluating the soft priorities of said plurality of CAM array blocks according to numeric significance so that matching entries in a first of said plurality of CAM array blocks are treated as having higher priority than matching entries in a second of said plurality of CAM array blocks when the soft priority of the first of said plurality of CAM array blocks is higher than the soft priority of the second of said plurality of CAM array blocks and vice versa when the soft priority of the second of said plurality of CAM array blocks is higher than the soft priority of the first of said plurality of CAM array blocks; and

means for identifying which of the matching CAM array blocks having the same soft priority has the higher hard priority.

23. (Currently amended) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks each including a plurality of rows of CAM cells; and

a hierarchical priority resolution circuit configured to identify a highest priority one of ~~a~~ the plurality of CAM array blocks having respective matching entries therein during a search operation by:

evaluating soft priorities of the plurality of CAM array blocks according to numeric significance so that matching entries in a first of said plurality of CAM array blocks are treated as having higher priority than matching entries in a second of said plurality of CAM array blocks when the soft priority of the first of said plurality of CAM array blocks is higher than the soft priority of the second of said plurality of CAM array blocks and vice versa when the soft priority of the second of said plurality of CAM array blocks is higher than the soft priority of the first of said plurality of CAM array blocks; and then

after completion of said evaluating soft priorities, evaluating competing hard priorities between at least two of the plurality of CAM array blocks having the same soft priorities, wherein each hard priority is a unique value indicative of the corresponding CAM array block's physical location relative to the other CAM array blocks, and each soft priority is an arbitrarily assigned value that is independent of the corresponding CAM array block's physical location.

24. (Currently amended) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks that each include a plurality of rows of CAM cells and that each have respective soft and hard priorities assigned thereto; and

a priority resolution circuit configured to resolve competing soft priorities for all possible combinations of soft priority order between said plurality of CAM array blocks and further configured to resolve competing hard priorities between at least two of said plurality of CAM array blocks having the same soft priority, during an operation to search the plurality of CAM array blocks to identify respective matching entries therein, wherein each hard priority is a unique value indicative of the corresponding CAM array block's physical location relative to the other CAM array blocks, and each soft priority is an arbitrarily assigned value that is independent of the corresponding CAM array block's

physical location.

25. (Original) The CAM device of Claim 24, wherein the CAM device comprises 2^{N+1} CAM array blocks therein, where N is an integer; and wherein said priority resolution circuit comprises $\log_2 N$ groups of precharged signal lines that are used during a priority resolution operation to resolve competing soft priorities between hit signals generated by said plurality of CAM array blocks.

26. (Original) The CAM device of Claim 24, wherein the CAM device comprises 2^{N+1} CAM array blocks, where N is an integer; and wherein said priority resolution circuit comprises $\log_2 N$ groups of N or N-1 precharged signal lines.

27. (Original) The CAM device of Claim 24, wherein the CAM device comprises $(2^x)^y$ CAM array blocks, where x and y are integers; and wherein said priority resolution circuit comprises y groups of precharged signal lines having 2^x or 2^x-1 signal lines per group.

28. (Original) The CAM device of Claim 27, wherein x and y represent a pair of integers selected from the pair groups (x,y) consisting of (3,3), (2,4) and (3,2).

29-58. (Canceled).

59. (New) The CAM device of Claim 1, wherein each row of CAM cells is coupled to a corresponding match line, and the CAM device further comprises:

a priority encoder coupled to the priority resolution circuit and configured to determine, for the CAM array block identified as having the highest soft and hard priorities, which row of CAM cells therein having an asserted match line has the highest priority.

60. (New) The CAM device of Claim 1, wherein the soft priorities are compared with each other.